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CENTRAL FAX CENTER**Docket No. 031948-8
Serial No. 10/782,826
Page 2**OCT 25 2006**IN THE SPECIFICATION:Page 1, 2nd paragraph after 2. Description of the Related Art

Conventional internal power supply circuits are described in, for example, Japanese Unexamined Patent Application Publication No. 5-314769 and Japanese Examined Patent Application Patent-Publication No. 7-13875. One conventional type of internal power supply circuit comprises a first voltage generator that generates a constant voltage V1 from the external power supply voltage VCC, a second voltage generator that outputs a variable voltage V2, and a voltage combiner that outputs the higher of the two voltages V1 and V2 as the internal power supply voltage VDD.

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In the second voltage generator, the external power supply voltage VCC is applied to a series circuit comprising one or more p-channel metal-oxide-semiconductor (PMOS) ~~transistor~~ transistors and a plurality of NMOS transistors. As the external power supply voltage VCC rises from the ground level, voltage V2 remains at the ground level until the external power supply voltage VCC is high enough to turn on the PMOS transistors, which operate as diodes. Voltage V2 then rises together with the external power supply voltage VCC, staying below the external power supply voltage VCC by a fixed amount equal to the PMOS transistor threshold voltage, or a multiple thereof.

Page 12, last paragraph on page.

When the external power supply voltage VCC is detected at some of the voltage detectors 10i as the external power supply voltage VCC rises, the detection signals from DETi from these voltage detectors 10i go high. The PMOS transistors 50i receiving the detection signals DETi at the high level are turned off and the corresponding PMOS transistors 49i cease to supply current, but the current supplying capability of the other

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PMOS transistors 49i 50i increases due to the rise in the external power supply voltage VCC,
so that the current supply to the internal circuits is not hindered.

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